

1ms-A' >

High Density Capacitor Using Topographic Surface

Background and Summary of the Invention

5 The present invention relates to integrated circuit structures and fabrication methods, and particularly to capacitor structures for mixed signal and analog applications.

Background

10 Many electronics applications require an integrated circuit that can accept analog signals as input, and process the information so that it can be communicated to another integrated circuit (IC) or user. This usually requires an analog interface on the IC and a digital core to perform signal processing and other digital functions.

15 For mixed signal product design, as the technology is scaled to smaller and smaller sized, capacitor size (such as a decoupling capacitor) does not decrease as quickly as some other technologies (such as interconnects and other components). Thus the total area occupied by the capacitor grows with respect to the other components and becomes substantially large in mixed signal design technologies, reaching areas of over 40% in some designs.

Density improvement for High Performance Capacitor Using Topographic Surface

20 The present application discloses an improved capacitor and fabrication method. The capacitor is formed over sections of the integrated circuit that have topographic or surface features which extend above and/or below the surface. Forming the capacitor on such

Brief Description of the Drawings

5 The disclosed inventions will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows a conventional capacitor structure.

Figure 2 shows a capacitor formed according to the present innovations.

10 **Figures 3a-3c** show partially fabricated capacitor structures at different stages of fabrication according to a preferred embodiment.

Figures 4a-4b show partially fabricated capacitor structures at different stages of fabrication according to the present innovations.

Figures 5a-5c show partially fabricated capacitor structures at different stages of fabrication according to a preferred embodiment.

Detailed Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of
5 embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

10 **Figure 1** shows a planar type capacitor. A top and side view are provided. The planar capacitor comprises a top plate **102** and a bottom plate **104**, with a dielectric material **106** sandwiched between. The plates are of course made from conductors, such as a metal or polysilicon.

15 **Figure 2** shows a topographic capacitor according to an embodiment of the present innovations. The top plate **202**, dielectric layer **204**, and bottom plate **206** are placed on surface features that extend above the planar surface, giving the deposited conductor and dielectric layers added surface area and increasing capacitor density.

20 The top plate and bottom plates are not planar, but instead have topographic features, or relief features extending above and/or below the surface, that increase the total surface area of the capacitor, thus increasing the total capacitance of the device. In this example, the capacitor is formed over marks placed on the wafer surface during the
25 alignment mark placement phase of processing. These marks in the preferred embodiment provide surface relief or three dimensional

features that extend out of and into the plane of the surface on which to form the capacitor, giving it dimension in the vertical direction as well as in the horizontal, as seen in the figure. Both the bottom and top plates are formed over these features, as is shown in the side view. The surface features, or relief features, may extend above the plane, recess into the plane, or both.

In existing processes, process steps are spent on adding alignment marks to the surface of the wafer. This existing process budget is used in the present preferred embodiment to also place features on the surface of the wafer where the capacitors are to be formed. These features provide the topography necessary for making a non-planar capacitor. The layout for placing the alignment marks can be modified to also place the topographic features in the same process steps, requiring modification only in the reticles and pattern layouts and not requiring added process steps. Of course other means can be used to place surface features upon which to form the innovative capacitors in less preferred embodiments. For example, scoring the surface of the wafer with a laser is one possible, though less preferred, alternative for placing relief features on the surface.

There are multiple ways that forming surface topographic features for the capacitors can be implemented into the process. Three example embodiments are discussed for integrating the capacitor formation into existing processes. The first example discusses forming surface features during the process phase in which the alignment marks are formed, called the pole 0 approach. The second example shows forming the surface features during the well oxidation phase, called the well oxidation approach. The third example shows a combination of

these two methods, in which the surface features are formed using both
aforementioned processes. These will each be discussed in further
detail separately below.

Figures 3a-3c show partially fabricated capacitor structures at
different stages within the pole 0 approach process flow. During this
phase of processing, the alignment marks are formed by etching the
wafer. **Figure 3a** shows a silicon surface with existing topographic or
relief features **302**. These features are formed on the semiconductor
surface using known means, such as masking and etching the silicon at
particular locations, followed by removal of the mask. In the preferred
embodiment, the features are formed in an existing process step
without adding a mask step to the process. The features are added
using only layout modification to the existing process flow.

Figure 3b shows the silicon substrate after formation of surface
features. The recesses seen here can be made about 5 angstroms deep.
A layer of field oxide **304**, or FOX, is deposited over the entire surface
in a thin layer. This layer insulates the capacitor from nearby devices.

Figure 3c shows the structure after the formation of the
capacitor. A bottom layer **306** for the capacitor is formed atop the FOX
layer. The bottom layer is a conducting material, preferably
polysilicon. The thickness of the bottom capacitor plate is about 3000A
on the bottoms of the topographic features and 3000A on the sidewalls.

A dielectric layer **308** is deposited on the bottom plate **306** by
means of CVD. In the preferred embodiment, the dielectric material
used is SiO_2 , Si_3N_4 , Ta_2O_5 , or Hf_2O_5 or a ferroelectric material such as
PZT or BST, and the layer is 100A to 1000A thick on the bottoms, and
the same thickness on the sidewalls of the topographic structures. Atop

Si₃N₄, Ta₂O₅, or Hf₂O₅ or a ferroelectric material such as PZT or BST, and is deposited by CVD to a thickness of about 100A to 1000A on the tops and sidewalls of the structure.

5 **Figures 5a-5c** show the formation of the innovative capacitor structure in the combined pole 0 and well oxidation approach process flow. This approach uses advantages of the two previously discussed examples to create surface features. In this variation, during the alignment mark placement phase of processing, the area where the capacitor is to be located is also patterned and etched, creating surface features during the step in which alignment marks are created. These are shown in **Figure 5a**.

10 The recesses made from this step are made deeper during the well preparation phase. The oxide layer that is formed during well oxidation is also formed in the capacitor's area, consuming some of the surface silicon. Thus, when this oxide is stripped, some silicon is also removed from the surface and the surface recesses for the capacitor are made deeper, allowing greater effective area for the capacitor plates. An additional 2-3 angstroms of depth can be added to the recesses with this method over the pole 0 process method alone (shown in **Figures**

15 **3**).

20 **Figure 5b** shows the surface after the field oxide has been formed. This oxide is subsequently stripped, deepening the recesses in the surface. **Figure 5c** shows the capacitor formed on the surface features.

25 Of course there are other methods that may be used to produce surface features upon which to form capacitors within the contemplation of the present application. Applying different methods

to the problem allows multiple choices for the design of the device,
which increases integration margin.

Definitions:

5 Following are short definitions of the usual meanings of some of
the technical terms which are used in the present application.
(However, those of ordinary skill will recognize whether the context
requires a different meaning.) Additional definitions can be found in
the standard technical dictionaries and journals.

10 **Relief Features:** features on the surface of a material that extend above
the surface plane or dip below it, or both. A non-planar surface.

Topographic features: relief features.

PZT: Lead zirconate-titanate, $\text{PbZrO}_3\text{TiO}_3$.

BST: Barium Strontium Titanate, $(\text{BaSr})\text{TiO}_3$.

Modifications and Variations

15 As will be recognized by those skilled in the art, the innovative
concepts described in the present application can be modified and
varied over a tremendous range of applications, and accordingly the
scope of patented subject matter is not limited by any of the specific
exemplary teachings given, but is only defined by the issued claims.

20 Additional general background, which help to show the knowl-

edge of those skilled in the art regarding variations and implementations of the disclosed inventions, may be found in the following documents, all of which are hereby incorporated by reference:

- 5 "Analog MOS Integrated Circuits, Part IV Successive Approximation and Parallel A/D and D/A converters," Ed. Paul Gray, David Hodges, Robert Broderon; (Wiley, 1980).

0998606-113001
FOOT " 9098650